Amendments to the Specification:

Please amend paragraphs 15, 36 and 39, and add two new paragraphs following paragraph 17, as follows:

Please amend paragraph 15 as follows:

[15] The k-node executes operating system instructions and manages operation of the ACE. The ~~k-mode~~ k-node is used to adapt other nodes to perform a function in much the same way that a subroutine may be called in a software program to perform a particular function. Further, the ~~k-mode~~ k-node, manages data flow between other nodes.

Please add the following paragraph after paragraph 17:

In one embodiment, an integrated circuit is provided. The integrated circuit comprises: a plurality of computational elements including a plurality of arithmetic nodes, a plurality of bit-manipulation nodes, a plurality of finite state machine nodes, and a plurality of input/output nodes; a first and a second processing node each having a core processor based on a common architecture, wherein the common architecture is reconfigurable to be a control node configured to control the interconnecting of said computational elements and a programmable scalar node (PSN) configured to perform computational applications; a first memory associated with said first processing node; a second memory associated with said second processing node; a first node wrapper for coupling said core processor of said first processing node to said first memory and to said computational elements; a second node wrapper for coupling said core processor of said second processing node to said second memory and to said computational elements; and means for interconnecting said computational elements and said first and second processing nodes to define a selected task to achieve a desired functionality, wherein the first processing node is configured as the control node based on a first configuration command, and the second processing node is configured as the PSN node based on a second configuration command.

Please add the following paragraph after paragraph 17:

In one embodiment, an adaptive computing engine is provided. The adaptive computing engine comprises: a first node having: a core processor reconfigurable into a controller node and a RISC processor, the controller node configured to execute operating system code and the RISC processor configured to execute application code; a memory for storing operating system executable code; means for transferring operating system executable code and data from said memory to said core processor, wherein the first node is configured as the controller node by a first configuration signal; a plurality of computational elements adapted to perform a selected function at least one of said computational elements having: a second node having: a core processor reconfigurable into a controller node and a RISC processor, the controller node configured to execute operating system code and the RISC processor configured to execute application code; a memory for storing application code; means for transferring application code and data from said memory to said second processor, wherein the second node is configured as the RISC processor by a second configuration signal; and a temporal interconnecting matrix coupling said controller node to said plurality of computational elements to perform a user selected function.

Please amend paragraph 36 as follows:

[36] ACE 200 further includes a k-node 224 coupled to MIN 214, which is also referred to the root level. An external memory controller 226 and host interface 228 are also connected to MIN 214. The k-node 224 receives instructions and configuration data from an external source such as a system controller (not shown) through host interface 228 upon startup or initiation of operation and then proceeds to adapt the nodes in each cluster 210 in accordance with configuration information. External memory controller 226 is adapted to interface with external memory, which may be DRAM, SRAM, Flash or any other volatile or non-volatile random access memory. In one preferred embodiment, k-node 224 is based on or similar in architecture to microprocessor-based ~~similar in architecture as microprocessor based~~ node 100 in that each includes a similar processor core 114. However, the k-node is adapted to execute operating system functions more efficiently. In another embodiment, the k-node is a PSN adapted to function as a k-node. Configuring the PSN is easily accomplished by setting a configuration register. When microprocessor based node 100 is configured as the k-node it executes boot code, operating system code and application code

rather than algorithms to implement specific functions or features. Regardless of the embodiment implemented on the integrated circuit, only one k-node is on each integrated circuit.

Please amend paragraph 39 as follows:

[39] Each node **202-206** and microprocessor based node and programmable scalar node **207** includes a number of computational elements and local memory surrounded by wrapper elements such as described in Figure **1**. Each node may be adapted on the fly to perform a desired function or to execute a specific algorithm.